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Lecture 15. GPUs, VLIW, Execution Models - Carnegie Mellon -

Computer Architecture 2015 - Onur Mutlu **Microprocessor**

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Examples of contemporary VLIW CPUs include the TriMedia media processors by NXP (formerly Philips Semiconductors), the Super Harvard Architecture Single-Chip Computer (SHARC) DSP

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Series in Microwave and Optical by Analog Devices, the C6000 digital signal processor (DSP) family by Texas Instruments, the ST200 family by STMicroelectronics based on the Lx architecture (designed in Josh Fisher's HP lab by Paolo Faraboschi), and the MPPA Manycore family by Kalray. These contemporary VLIW CPUs are mainly successful as embedded ...

## **Very long instruction word - Wikipedia**

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Computer Architecture ABSTRACT VLIW architectures are distinct from traditional RISC and CISC architectures implemented in current mass-market microprocessors. It is important to distinguish instruction-set architecture—the processor programming model—from implementation—the physical chip and its characteristics. VLIW microprocessors and superscalar implementations of traditional

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## **An Introduction To Very-Long Instruction Word (VLIW ...**

VLIW Architecture. Very-Long Instruction Word (VLIW) architectures are a suitable alternative for exploiting instruction-level parallelism (ILP) in programs, that is, for executing more than one basic (primitive) instruction at a time. These processors contain multiple functional units, fetch from the instruction cache a Very-Long Instruction Word containing several primitive instructions, and dispatch the entire VLIW for parallel execution.

### **VLIW Architecture - IBM**

Introduction o Very long instruction word or VLIW refers to a processor architecture designed to take advantage of instruction level parallelism o Instruction of a VLIW processor consists of



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multiple independent operations grouped together. o There are Multiple Independent Functional Units in VLIW processor architecture. o Each operation in the instruction is aligned to a functional unit. o All functional units share the use of a common large register file. o This type of processor ...

## **VLIW Processors - SlideShare**

- change in the instruction set architecture, i.e., 1 program counter points to 1 bundle (not 1 operation)
- want operations in a bundle to issue in parallel
- fixed format so could decode operations in parallel
- enough FUs for types of operations that can issue in parallel
- pipelined FUs

Autumn 2006 CSE P548 - VLIW 2 VLIW Processors

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## **VLIW Processors - [courses.cs.washington.edu](https://courses.cs.washington.edu)**

In computer architecture, a transport triggered architecture (TTA) is a kind of processor design in which programs directly control the internal transport buses of a processor. Computation happens as a side effect of data transports: writing data into a triggering port of a functional unit triggers the functional unit to start a computation. This is similar to what happens in a systolic array.

## **Transport triggered architecture - Wikipedia**

Advantages of Superscalar Architecture : In a Superscalar Processor, the detrimental effect on performance of various hazards becomes even more pronounced. The compiler can avoid many hazards through judicious selection and ordering of instructions.

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## **Superscalar Architecture - GeeksforGeeks**

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WhatIs.com. Very long instruction word (VLIW) describes a computer processing architecture in which a language compiler or pre-processor breaks program instruction down into basic operations that can be performed by the processor in parallel (that is, at the same time). These operations are put into a very long instruction word which the processor can then take apart without further analysis, handing each operation to an appropriate functional unit.

## **What is VLIW (very long instruction word)? - Definition ...**

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Lesson. Quiz & Worksheet - Superscalar & VLIW Architectures. Quiz. Course. Try it risk-free for 30 days. Instructor: Abirami Thangavel. I have been teaching Computer Science for college students ...

## **Superscalar & VLIW Architectures: Characteristics ...**

VLIW Introduction Superscalar Control Logic Scaling Each issued instruction must be checked against  $W \times L$  instructions, i.e., the growth in hardware ?  $W \times (W \times L)$  For inorder machines, L is related

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to pipeline latencies For outoforder machines, L also includes time spent in instruction buffers (instruction window or ROB)

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